Turbo Codes and Turbo Decoders for Deep Space Communications

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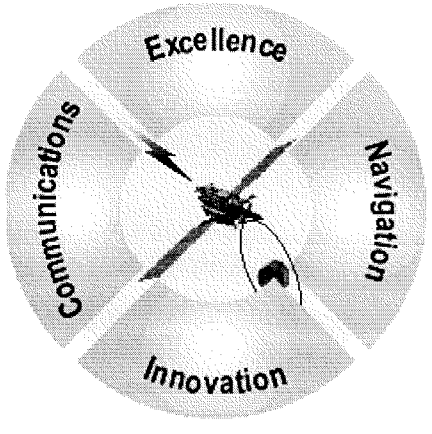

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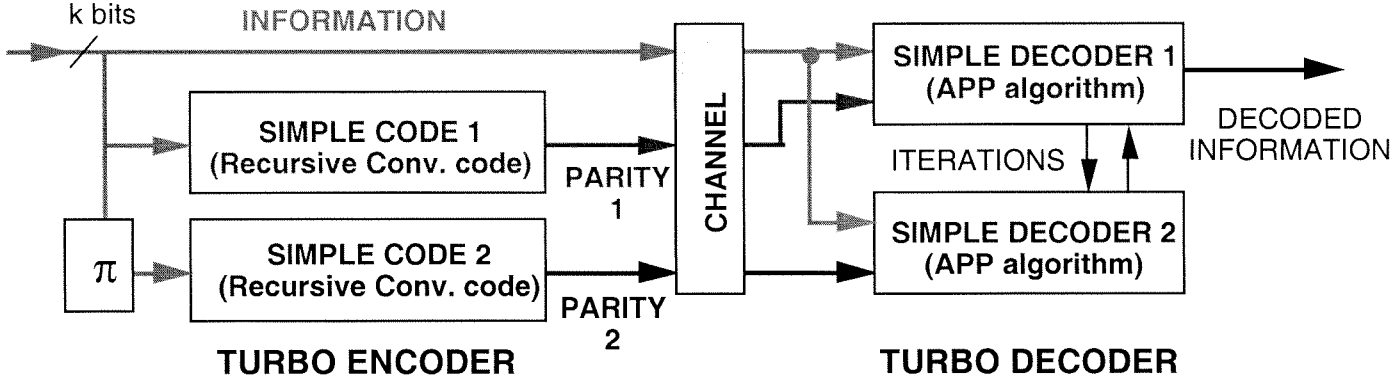
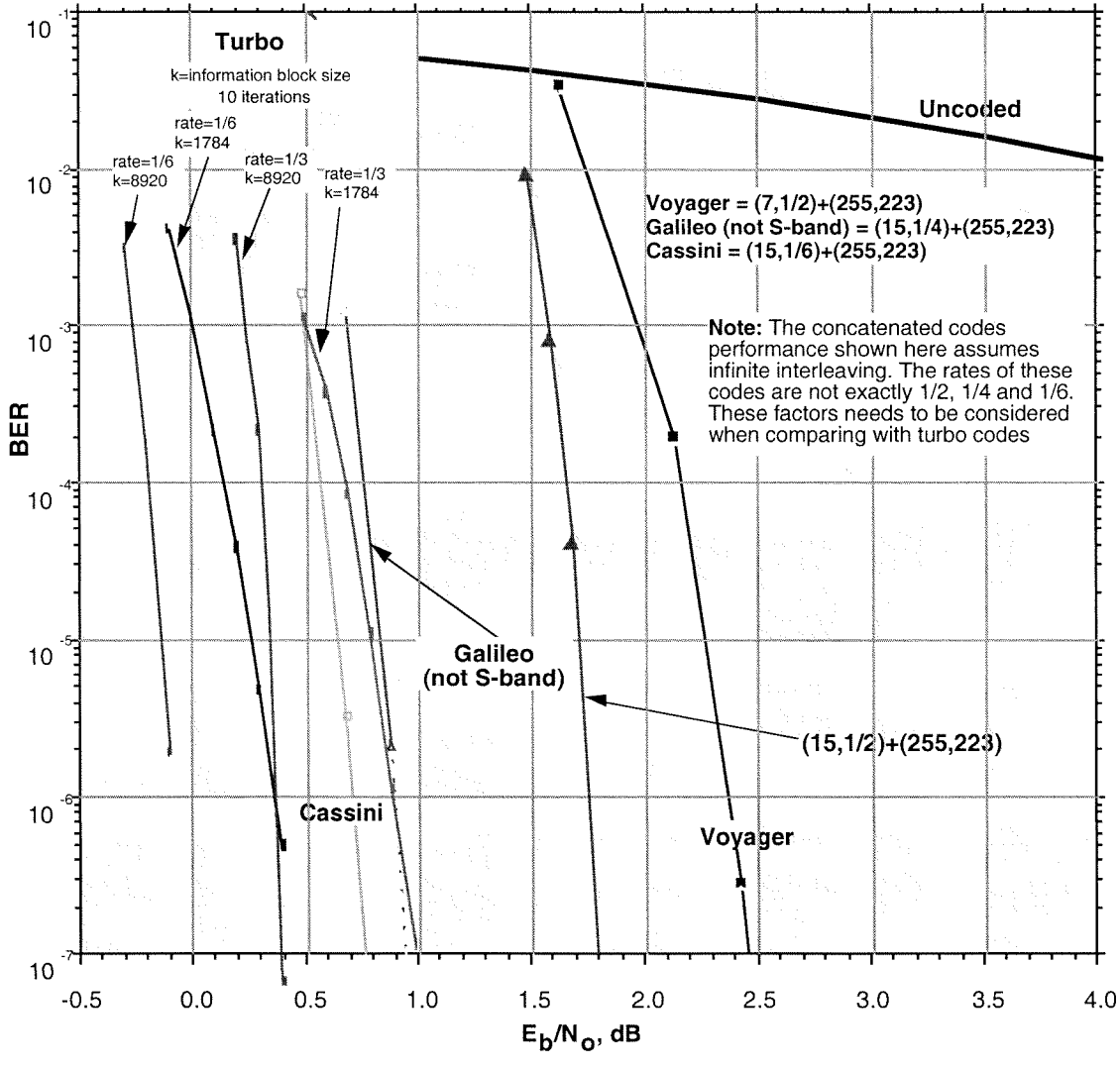
TURBO ENCODER AND DECODER

- For a block of k information bits, each constituent code generates a set of parity bits. The turbo code consists of the information bits and both sets of parity.
- The key innovation is the interleaver π preceding the second encoding.

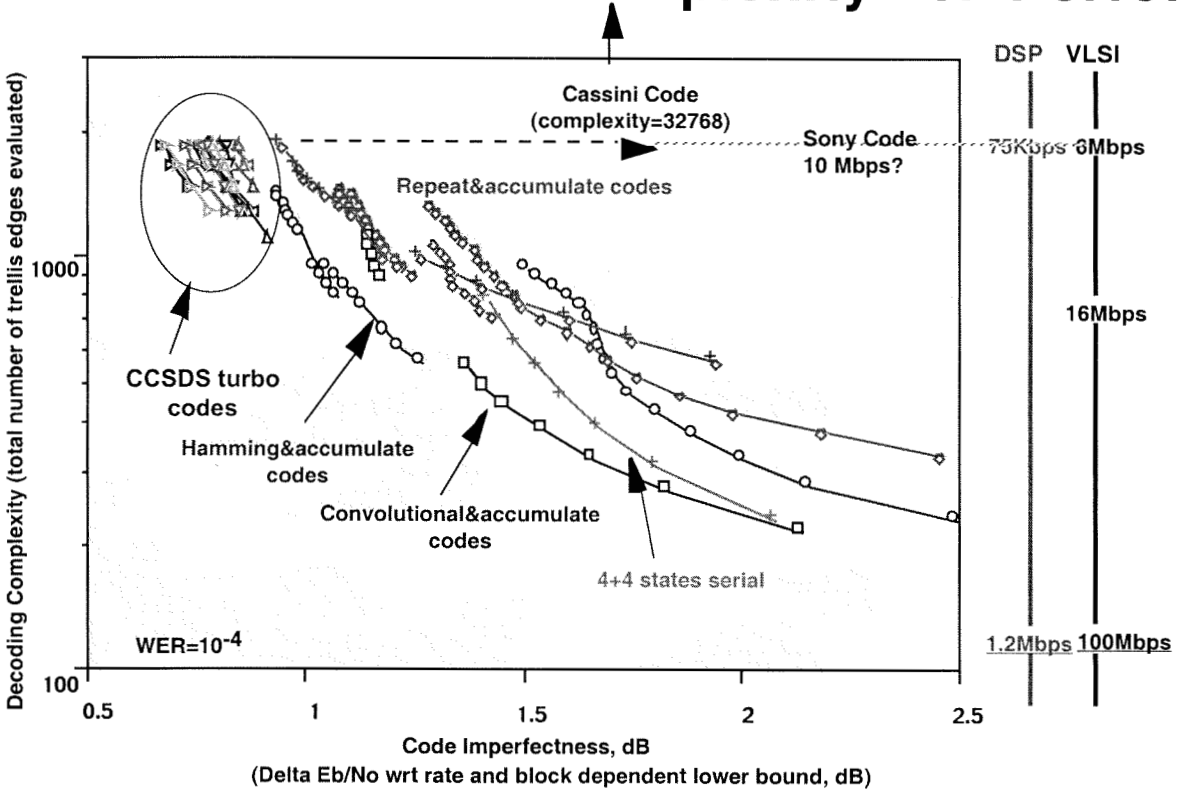


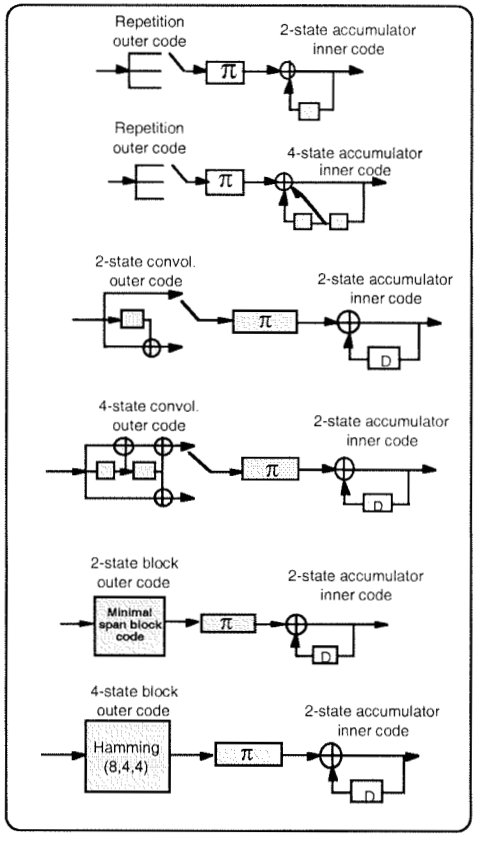
- Each decoder uses the APP algorithm to form likelihood estimates of the decoded bits, then sends these (soft) estimates to the other decoder, in the form of "extrinsic information".
- The overall turbo decoder iterates between the outputs of the individual decoders until satisfactory convergence is reached.

PERFORMANCE COMPARISON



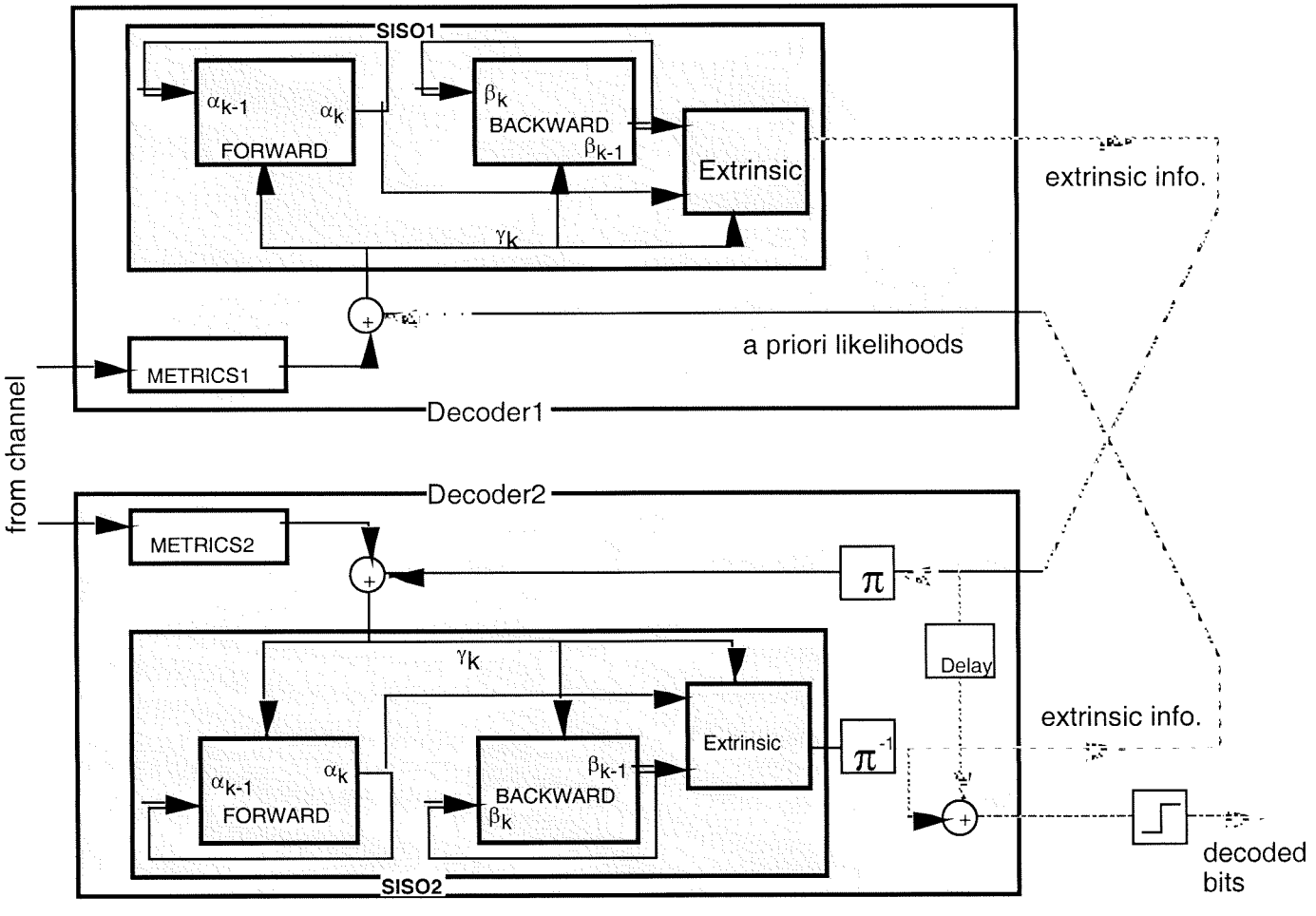
Code Complexity vs. Performance





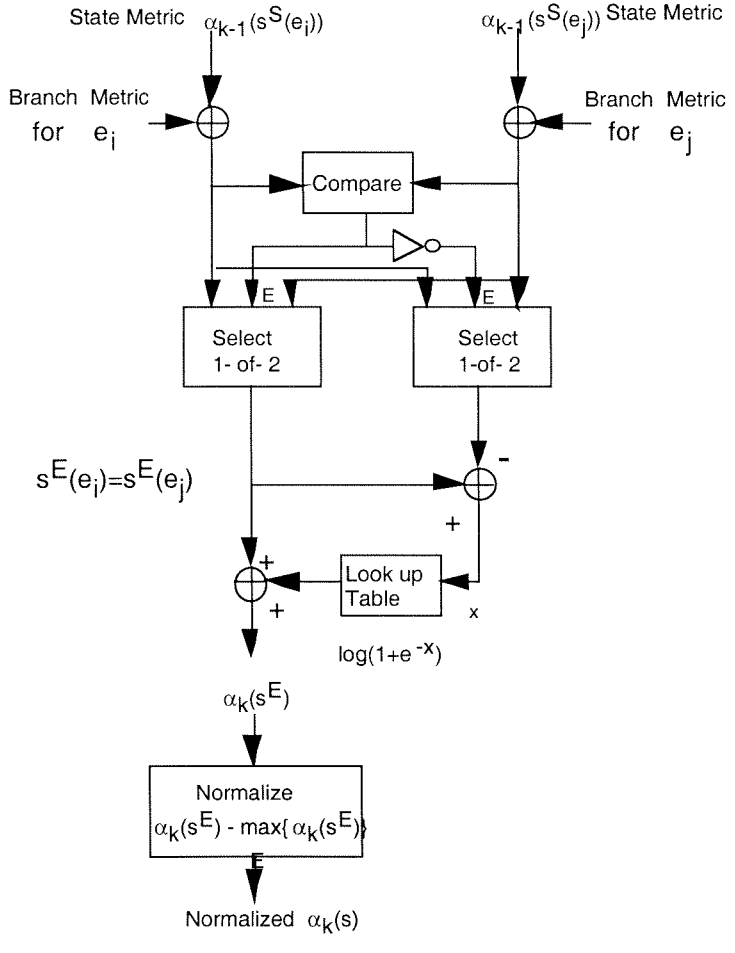
- **Tabulated complexity and performance data for CCSDS turbo codes and several turbo-like codes with extremely simple structure**
  - **Complexity measure = total trellis edges evaluated (forward, backward, extrinsics)**
    - **reflects both structural complexity and iterative complexity**
    - **is approximately technology-independent**
  - **Graph shows tradeoffs possible with different classes of codes and estimated decoding speed with current DSP and VLSI technology**

General Structure of the Turbo Decoder

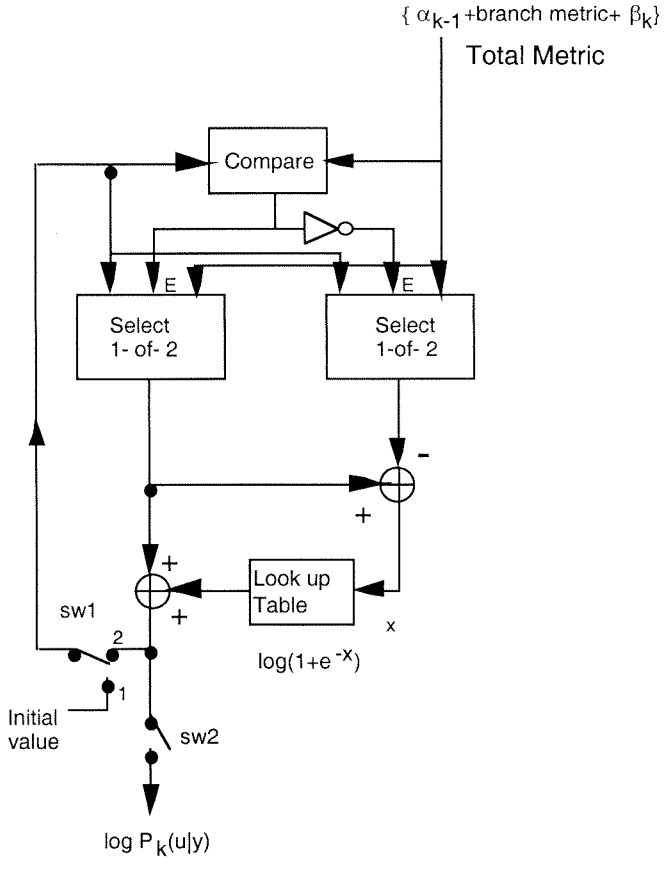


SISO = "soft-input, soft-output" module

Basic Circuits to Implement the SISO Algorithm



Basic Structure for Forward and Backward Computation in the SISO Algorithm



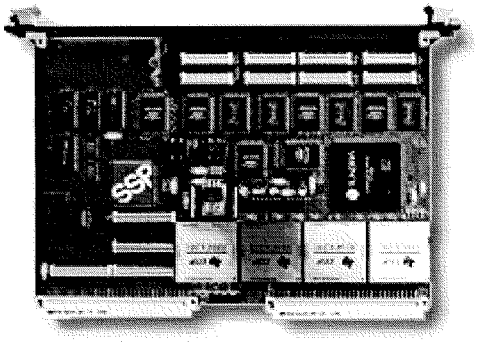
Basic Structure for Computation of Extrinsics in the SISO Algorithm

DSN TURBO DECODER IMPLEMENTATION

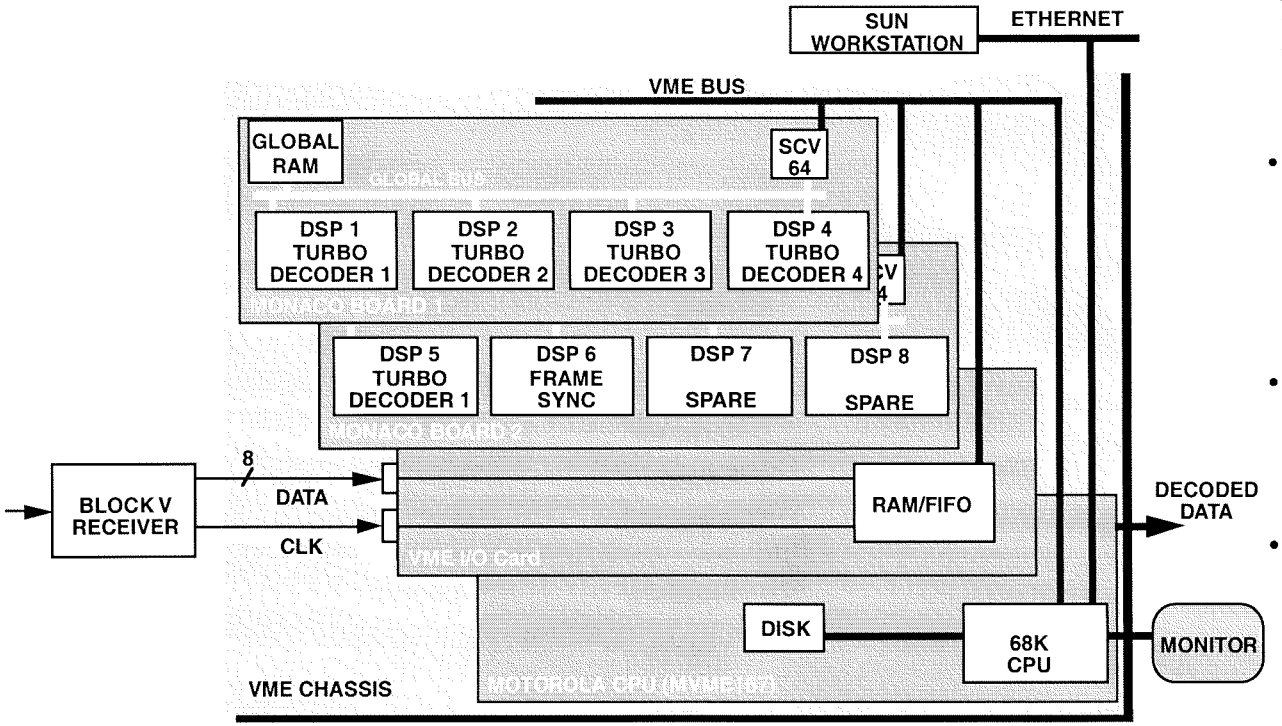
- TURBO CODES ARE BLOCK CODES (LIKE REED-SOLOMON CODES)
  - DECODING REQUIRES FRAME SYNCHRONIZATION BEFORE DECODING
  - FRAME SYNC IS DONE ON SYMBOLS, NOT BITS
- TURBO DECODING BEING IMPLEMENTED ON COMMERCIAL VME BOARDS, WITH 4 DSP PROCESSORS PER BOARD
  - ONE PROCESSOR DECODES ONE TURBO CODE BLOCK AT A TIME
  - SYSTEM WILL HAVE
    - 5 PROCESSORS DOING DECODING
    - 1 PROCESSOR FOR FRAME SYNC
    - 2 PROCESSORS FOR SPARES
- WE ARE DEVELOPING A 50 kbps DECODER ON ONE PROCESSOR
  - TOTAL SYSTEM SPEED WILL BE 250 kbps
  - DEMO WITH STM IN DTF-21 IN SPRING, 2000

Turbo Decoder Development

- Continued development of prototype turbo decoder for DSN
  - Motorola CPU running under Vx-Works in VME chassis
  - 4-DSP board (Monaco board by Spectrum, Inc.) in VME chassis
- Developed software for communicating with the DSP board
- Developed "C" language decoder to be used for assembler verification (with sliding window, to reduce memory rqmts.)



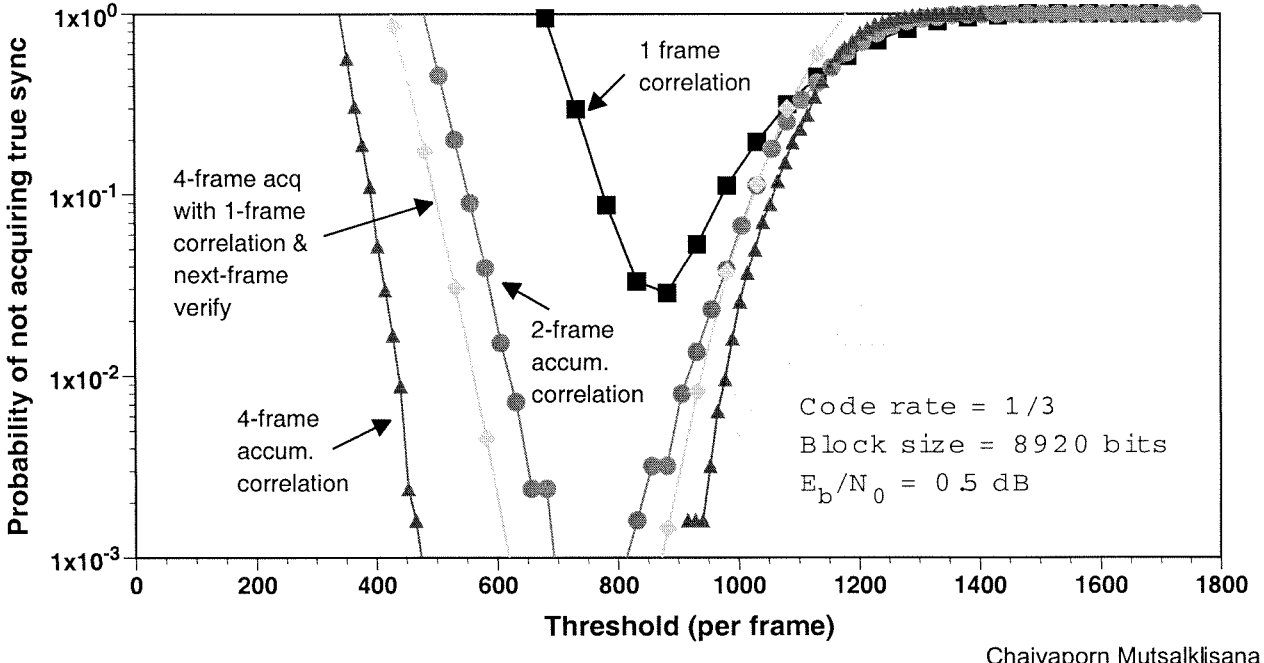
Monaco Board: 4-DSPs; 8 ALUs per DSP



- Developed Vx-works code for I/O and testing
  - This reads a sequence of windows of symbols from a file using a handshake
- Made progress in developing a faster I/O method, using the VME SCV64 controller
- Tested DSP's DMA to off-chip memory

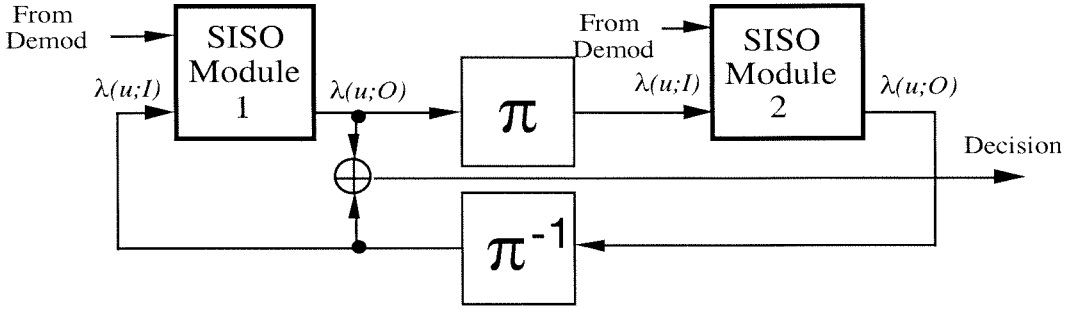
Frame Synchronizer

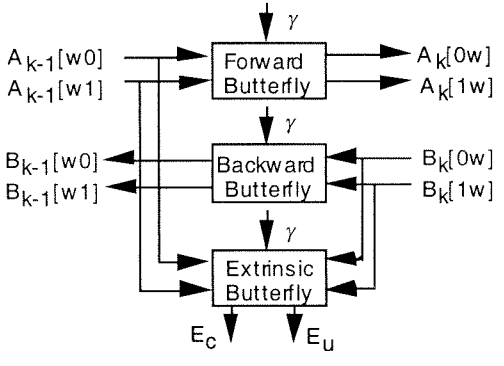
- Length of sync marker in channel-symbol domain varies with code rate
  - marker length is 64, 96, 128, or 192 bits, for rate 1/2, 1/3, 1/4, or 1/6, respectively
- Developed "C" program for symbol-domain frame sync
- Verified that 96-bit correlation (rate 1/3) is feasible for DSP at required bit rate
- Analyzed synchronizer performance for 4 schemes for rate-1/3 code
  - acquisition in one frame
  - acquisition in two frames using accumulated correlations
  - acquisition in four frames using accumulated correlations
  - acquisition within four frames using one-frame correlations with next-frame verification



ASIC TURBO DECODER

- ASIC SISO modules will be universal building blocks for:
  - Fast/parallel decoders
  - Parallel, serial, TCM configurations, etc.

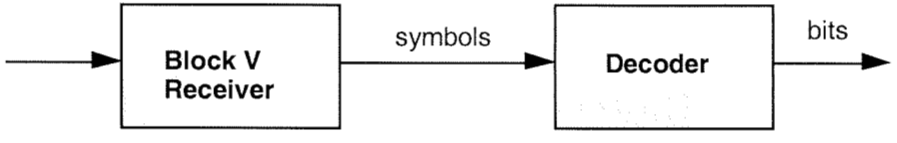




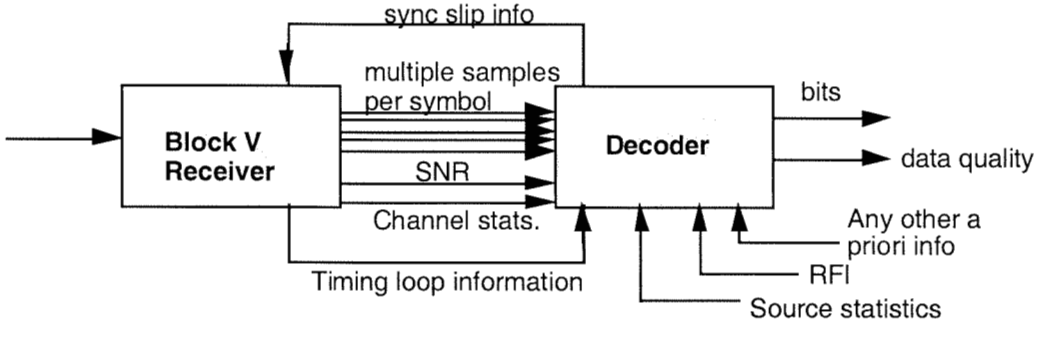
- SISO parallel architecture for ASIC. The SISO operates on a trellis representing the encoder structure. In order to implement the SISO module as an ASIC we take the following approach to generate a highly parallel architecture and to simplify the layout process for ASIC implementation:
- Partition trellis sections into butterflies. Each butterfly performs a portion of the three computations required by the SISO module, namely forward, backward and extrinsic.
- Connect these butterflies as a building block.
  - Integrate the building blocks to construct the trellis section.
  - Pipeline trellis sections to construct the SISO module.
  - Interconnect the SISO modules, according to the permutation, to construct the turbo decoder. The interconnected SISO circuits exchange messages, at each iteration, corresponding to the extrinsics.

Coupled Receiver/Decoder

- Improvements in decoder performance
  - more accurate SNR estimates computed from multiple samples per code symbol
- Improvements in decoder performance and receiver synchronization
  - receiver supplies the decoder with multiple samples per code symbol to counteract situations when the symbol boundaries are not precisely aligned by the receiver
  - Algorithms for the decoder to detect and locate places where symbol insertions or deletions occur
  - use this information to improve chances of correctly decoding most of the code blocks with sync slips
  - assist the receiver in correcting its symbol frequency to prevent further slips
- Algorithms for supplying and utilizing information fed back from the decoder to the receiver to improve its synchronization loops



Current receivers and decoders share information via a simple unidirectional interface



Coupled receiver/decoder shares information bi-directionally.
(Decoder also accepts variuos kinds of a priori information)